reference discloses all the claimed elements in isolation. Rather, "[a]nticipation requires the presence in a single prior reference disclosure of each and every element of the claimed invention, *arranged as in the claim*." *Lindemann Maschinenfabrik GmbH v. American Hoist & Derrick Co.*, 730 F.2d 1452, 221 USPQ 481, 485 (Fed. Cir. 1984) (citing *Connell v. Sears, Roebuck & Co.*, 722 F.2d 1542, 220 USPQ 193 (Fed. Cir. 1983)) (emphasis added).

Prior art Figure 1 of the instant application shows a memory device 100 in which memory cells are arranged in rows and columns. Each column is shown as a vertical strip of memory cells, and each row is shown as a horizontal strip of memory cells. Within memory device 100, each column corresponds to a single bank of memory cores. For example, memory cores 120, 124, and 128 of strip 102 are part of Bank 0, and memory cores 130, 134, and 136 of strip 104 are part of Bank 1. **Memory device 100 does not show memory cores from two banks "interleaved" or "alternating" in a single strip. Nor does memory device 100 show sense amplifiers shared among memory cores from two banks that are interleaved or alternating in a single strip.**

Referring now to the claims, applicants respectfully submit that a proper *prima facie* case of anticipation has not been established because prior art Figures 1 and 2 do not disclose "each and every element of the claimed invention, arranged as in the claim," as required by the federal circuit. Specific examples of non-anticipated claimed subject matter from the independent claims are now described.

With respect to independent claim 1, applicants respectfully submit that prior art Figures 1 and 2 do not disclose, teach, or suggest the subject matter of claim 1, including for example, "wherein the memory cores from two of the different ones of the plurality of banks are interleaved in a strip with the plurality of shared sense amplifiers."

With respect to independent claim 5, applicants respectfully submit that prior art Figures 1 and 2 do not disclose, teach, or suggest the subject matter of claim 5, including for example, "wherein the memory cores of the two of the plurality of banks are interleaved in a row."

With respect to independent claim 9, applicants respectfully submit that prior art Figures 1 and 2 do not disclose, teach, or suggest the subject matter of claim 9, including for example, "a second bank of memory cores interleaved with the first bank of memory cores arranged in the

strip."

With respect to independent claim 14, applicants respectfully submit that prior art Figures 1 and 2 do not disclose, teach, or suggest the subject matter of claim 14, including for example, "a second bank of memory cores interleaved with the first bank of memory cores arranged in the strip."

With respect to independent claim 18, applicants respectfully submit that prior art Figures 1 and 2 do not disclose, teach, or suggest the subject matter of claim 18, including for example, "wherein a strip of memory cores in the first dimension includes memory cores from a first bank interleaved with memory cores from a second bank."

With respect to independent claim 22, applicants respectfully submit that prior art Figures 1 and 2 do not disclose, teach, or suggest the subject matter of claim 22, including for example, " wherein a strip of memory cores in the first dimension includes memory cores from a first bank interleaved with memory cores from a second bank."

With respect to independent claim 26, applicants respectfully submit that prior art Figures 1 and 2 do not disclose, teach, or suggest the subject matter of claim 26, including for example, "wherein a strip of memory cores in the first dimension includes memory cores from a first bank interleaved with memory cores from a second bank."

With respect to independent claim 29, applicants respectfully submit that prior art Figures 1 and 2 do not disclose, teach, or suggest the subject matter of claim 29, including for example, "wherein the first bank of memory cores and the second bank of memory cores are interleaved in a first row on the memory device."

With respect to independent claim 33, applicants respectfully submit that prior art Figures 1 and 2 do not disclose, teach, or suggest the subject matter of claim 33, including for example, "a second bank of memory cores, wherein the first bank of memory cores and the second bank of memory cores are interleaved in a first row on the memory device."

With respect to independent claim 36, applicants respectfully submit that prior art Figures 1 and 2 do not disclose, teach, or suggest the subject matter of claim 36, including for example, "wherein memory cores arranged in a first row alternate between a first bank and a second bank."

With respect to independent claim 40, applicants respectfully submit that prior art Figures 1 and 2 do not disclose, teach, or suggest the subject matter of claim 40, including for example, "a plurality of memory cores physically arranged in rows and columns and logically arranged into banks that share sense amplifiers, wherein memory cores arranged in a first row alternate between a first bank and a second bank."

With respect to independent claim 43, applicants respectfully submit that prior art Figures 1 and 2 do not disclose, teach, or suggest the subject matter of claim 43, including for example, "wherein memory cores arranged in each of the plurality of rows alternate between two banks, and memory cores arranged in each of the plurality of columns are from a different bank."

With respect to independent claim 46, applicants respectfully submit that prior art Figures 1 and 2 do not disclose, teach, or suggest the subject matter of claim 46, including for example, "a plurality of sense amplifiers positioned between memory cores within each row, wherein every other memory core within each row is assigned to a bank."

With respect to independent claim 49, applicants respectfully submit that prior art Figures 1 and 2 do not disclose, teach, or suggest the subject matter of claim 49, including for example, "a second bank of memory cores interleaved with the first bank of memory cores in the first row."

With respect to independent claim 52, applicants respectfully submit that prior art Figures 1 and 2 do not disclose, teach, or suggest the subject matter of claim 52, including for example, "wherein the first bank of memory cores and the second bank of memory cores are arranged in a strip with the plurality of sense amplifiers."

With respect to independent claim 55, applicants respectfully submit that prior art Figures 1 and 2 do not disclose, teach, or suggest the subject matter of claim 55, including for example, "a plurality of memory cores logically arranged into Rambus-compatible banks and physically arranged into rows and columns, wherein each column includes interleaved memory cores from two different Rambus-compatible banks."

Conclusion

Applicant respectfully submits that the claims are in condition for allowance and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's attorney (612-371-2159) to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

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CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Commissioner of Patents, Washington, D.C. 20231, on this 11th day of September, 2002.

Name Amy Moriarty Signature Amy Moriarty